## EMILIO G. COTA

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education	Columbia University (New York, NY, USA)		
	Ph.D. in Computer Science	May 2019	
	"Scalable Emulation of Heterogeneous Systems." Advisor: Prof. Luca Carloni		
	M.S. in Computer Science	May 2012	
	University of Seville (Seville, Spain) – with 5 <sup>th</sup> year at Imperial College (London, UK)		
	Industrial Engineer, "Ingeniero Industrial, Intensificación Electrónica"	June 2008	
	"Autonomous Navigation of a Simple Mobile-Robot." Advisors: Prof. A. Astolfi, Dr. P.D. Mitcheson		
experience	<b>Google LLC (New York, NY, USA),</b> <i>Software Engineer</i> <i>2021—:</i> MLIR-based compilers for ML workloads running on CPU. <i>2019—2021:</i> Distributed systems for structured search.	2019—	
	<b>Columbia University (New York, NY, USA),</b> <i>Graduate Research Assistant</i> 2010–2019 <i>Computer architecture research</i> on hardware accelerators. Quantified the importance of private local memories for accelerator performance. Devised a technique to reuse these private memories to expand the last-level cache when the accelerators are otherwise inactive. Wrote an architec- tural simulator to evaluate these ideas.		
	<i>Software systems research</i> on fast, scalable cross-ISA machine emulation and instrume multi-cores. Most of the resulting implementation is in <i>upstream</i> QEMU (300+ comm lights: scalable dynamic binary translation and subsequent execution (after this work	<i>systems research</i> on fast, scalable cross-ISA machine emulation and instrumentation for es. Most of the resulting implementation is in <i>upstream</i> QEMU (300+ commits). High- alable dynamic binary translation and subsequent execution (after this work, cross-ISA	

scalability is similar to that with KVM) while using a shared code cache and correctly handling guest-host differences in atomic instructions (i.e., LL/SC on CAS hosts), scalable hash table (QHT), scalable lock profiler, fast guest instrumentation, fast and correct cross-ISA FP emulation (2×+ SPECfp06 average speedup) by selectively leveraging the host FPU, dynamic TLB resizing (1.8× SPECint06 speedup), indirect branch handling improvements (1.3× SPECint06 speedup).

**CERN (Geneva, Switzerland),** *Junior Fellow* 2008–2010 Wrote Linux kernel drivers for custom and commercial devices, including the VME bus, whose driver was eventually merged into mainline Linux. Developed an event logging infrastructure and an automated testbed to validate the LHC's Central Timing system. Wrote kernel and userspace software for the original White Rabbit slave nodes.

skills Systems programming: C, C++, multi-core scalability, performance optimization, Linux kernel hacking, MLIR, LLVM.

Development: git, Perl and Python scripting.

## publications Cross-ISA Machine Instrumentation using Fast and Scalable Dynamic Binary Translation

Emilio G. Cota, Luca P. Carloni. Intl. Conf. on Virtual Execution Environments (VEE), 2019. Cross-ISA Machine Emulation for Multicores

Emilio G. Cota, Paolo Bonzini, Alex Bennée, Luca P. Carloni.

Intl. Symp. on Code Generation and Optimization (CGO), 2017.

Handling Large Data Sets for High-performance Embedded Applications in Heterogeneous Systems-on-chip

Paolo Mantovani, Emilio G. Cota, Christian Pilato, Giuseppe Di Guglielmo, Luca P. Carloni. *Intl. Conf. on Compilers, Architectures and Synthesis for Embedded Systems (CASES), 2016.* 

An FPGA-Based Infrastructure for Fine-Grained DVFS Analysis in High-Performance Embedded Systems

Paolo Mantovani, Emilio G. Cota, Kevin Tien, Christian Pilato, Giuseppe Di Guglielmo, Ken Shepard, Luca P. Carloni.

Design Automation Conference (DAC), 2016.

Exploiting Private Local Memories to Reduce the Opportunity Cost of Accelerator Integration

Emilio G. Cota, Paolo Mantovani, Luca P. Carloni. Intl. Conf. on Supercomputing (ICS), 2016.

An Analysis of Accelerator Coupling in Heterogeneous Architectures Emilio G. Cota, Paolo Mantovani, Giuseppe Di Guglielmo, Luca P. Carloni. Design Automation Conference (DAC), 2015.

Accelerator Memory Reuse in the Dark Silicon Era Emilio G. Cota, Paolo Mantovani, Michele Petracca, Mario R. Casu, Luca P. Carloni. *Computer Architecture Letters, Jan. 2014.* 

teachingTeaching Assistant, Computer ArchitectureFall 2011, Fall 2012, Summer 2018Assisted with teaching, lab grading and final project design of Columbia's graduate computer<br/>architecture course (CSEE4824).

honors Extraordinary Teaching Assistant Award from Columbia Engineering Fall 2011